RADIO RECEIVER CIRCUITS

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RF STAGE AND RF AMPLIFIERS

Almost every radio receiver has an RF stage, which consists of a tunable circuit and an RF amplifier that are connected to the terminals of the antenna. In some receivers the RF amplifier is omitted and the RF stage only consists of a tunable circuit that is connected to the antenna. However, these receivers can only be used in high-signal strength areas. The receiver with a RF amplifier has a superior performance than the one without RF amplifier and can it can be used anywhere in the world.

The RF stage is mainly responsible for selecting and amplifying the required signal (channel or station) while rejecting all other frequencies. The tuned circuit provides the bandpass response needed for front-end selectivity while the amplifier provides amplification needed to improve the sensitivity of the receiver. Additional to improving of sensitivity and selectivity of the receiver, the RF stage is also responsible for the following:

- Prevention of image frequency and other spurious frequencies from entering the mixer and heterodyning there to produce an interfering frequency equal to intermediate frequency (IF) from the desired signal.
- Prevention of reradiation of the local oscillator output frequency through the receiving antenna.
- Providing better coupling of the receiver to the antenna.
- Improve signal-to-noise ratio of the receiver.

Tuned Radio Frequency Amplifier

RF amplifiers are amplifiers that are designed to operate at radio frequencies. They are used in both transmitters and receivers to provide amplification. In transmitters RF amplifiers are used in the power amplifier (PA) stage to amplify the modulated signal before it is applied to the antenna, while in receivers RF amplifiers are used in the RF stage to improve the sensitivity of the receiver, and in the IF stage to provide the bulk of receiver amplification. These RF amplifiers are tuned, transformer-coupled amplifiers. The tuned circuit is a parallel resonant circuit that is connected to the collector or drain of the amplifying BJT transistor or FET transistor, which is used to provide the bandpass response. The amplifier may be single or double tuned. In the former, either primary or secondary is tuned, while in the latter, both the primary and secondary are tuned.

A small signal primary-tuned RF amplifier circuit is shown in Figure 1a. However, at radio frequencies, inter-electrode (between terminals) parasitic capacitance will develop between the base and collector (C_{BC}), base and emitter (C_{BE}) and between the collector and emitter (C_{CE}). Since C_E is a large capacitor, it can be replaced by a short circuit at high frequency, thus resulting in C_{CE} appearing as if it is between the collector and ground. In most cases C_{CE} is represented as stray capacitance (C_S), as shown in Figure 1b.

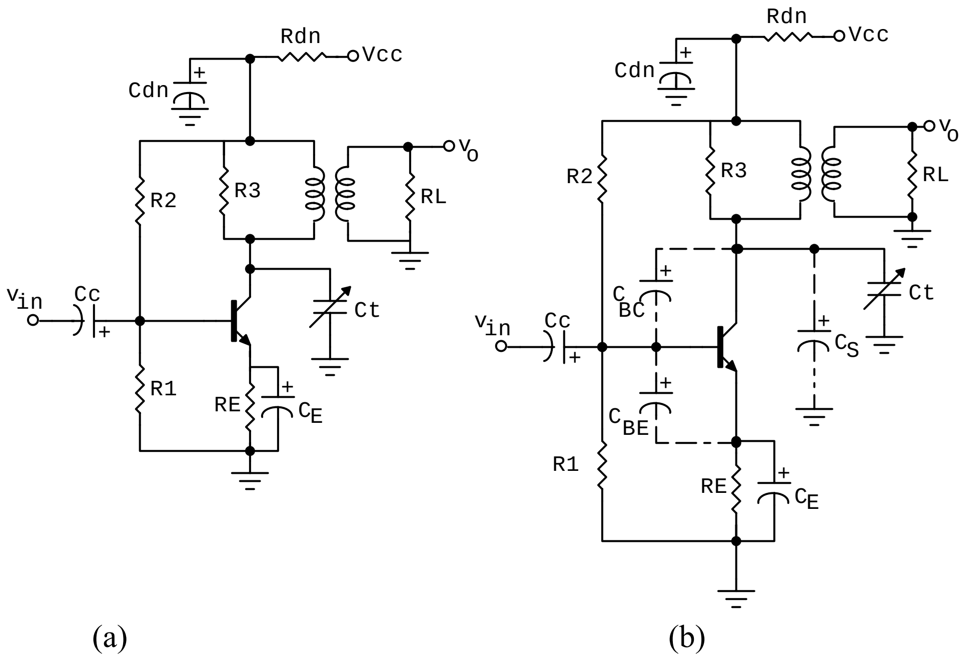


Figure 1 Small signal RF amplifier

Parasitic capacitance C_s provides shunt capacitance that will drastically reduce the gain of the amplifier at RF frequencies. To counter this problem, the collector resistor is replaced by a tuned network and then transformer-coupling to the next stage. Parallel-resonating the collector circuit helps to produce a high impedance so to maintain high gain even at RF frequencies. Resistor R_{dn} and capacitance C_{dn} form a low-pass filter called *decoupling network*, which provides isolation between the circuit and power supply, and possible feedback to other circuits. The value of R_{dn} is chosen to be about 100 Ω so as to ensure that the voltage drop across it is negligible small (less than 0.1 V). The tank resistor R_3 is included across the primary of the coupling transformer in order to increase bandwidth and to reduce the effect of the circuit parasitics. The analysis of the circuit is a follows:

The input voltage v_i produces a base current

$$i_b = \frac{v_{in}}{R_{in}} = \frac{v_{in}}{(1+\beta)r_e}$$

Where r_e is the effective dynamic resistance of the emitter junction, which is the ratio of the junction potential (V_T) to the emitter current I_E, and V_T varies between 25 and 40 mV depending on the base-emitter junction geometry. That is,

$$r_e = \frac{V_T}{I_E}$$

After amplification the input voltage will produce collector voltage v_c, which is given by

$$v_c = i_c Z_c$$

where Z_c is the effective ac impedance from collector to ground.

The gain will be

$$A_v = -\frac{v_c}{v_{in}} = -\frac{i_c Z_c}{i_b R_{in}}$$

Substituting for i_c and R_{in} we get

$$A_v = -\frac{\beta i_b Z_c}{i_b(1+\beta)r_e} = -\frac{\beta}{(1+\beta)}\frac{Z_c}{r_e} = -\alpha\frac{Z_c}{r_e} \approx -\frac{Z_c}{r_e}$$

The maximum gain will occur when the tuned circuit is at resonance and is given by

$$A_{vo} = -\frac{R_c^{'}}{r_e}$$

Where $R_c^{'}$ is the entire tank loading, which is given by

$$R_c^{'} = \frac{r_c}{2}$$

Where r_c is the collector dynamic impedance, and in cases where r_c is not given $R_c^{'}$ can be determined by

$$R_c^{'} = R_3 // R^{'}{}_L // R_{coil}$$

Where $R^{'}{}_L = \left(\frac{n_p}{n_s}\right)^2 R_L = a^2 R_L$ and $R_{coil} = Q_u X_L$

The resonant frequency is given by

$$f_o = \frac{1}{2\pi\sqrt{L_P C_T}}, \text{ where } C_T = C_t + C_S + C_{BC}$$

And the bandwidth of the circuit is given by

$$BW = \frac{f_o}{Q_L}$$

Where Q_L is the effective or loaded Q of the circuit, which is given by

$$Q_L = \frac{R_c^{'}}{X_L}$$

Since the circuit uses transformer coupling, the final output voltage v_o will be

$$v_o = \left(\frac{n_s}{n_p}\right) v_c$$

Therefore, the overall gain of the circuit will be

$$A_{vT} = -\frac{v_o}{v_{in}} = -\frac{\left(\frac{n_s}{n_p}\right) v_c}{v_{in}} = -\left(\frac{n_s}{n_p}\right) A_{vo}$$

In dB, the gain is

$$A_{vT}(dB) = 20\log(A_{vT})$$

Example 1: For the small-signal RF amplifier shown in Figure 1, if $V_{cc} = 15\ V$; $v_i = 50\ mV$; $V_T = 26\ mV$; $Q_u = 75$; $L_s = 18\ \mu H$; $n_p/n_s = 10$; $k = 1$; $R_1 = 3.9\ k\Omega$; $R_2 = 18\ k\Omega$; $R_E = 1.2\ k\Omega$; $R_3 = 5\ k\Omega$; $R_L = 50\ \Omega$; $C_{BC} = 2.5\ pF$; $C_s = 3.5\ pF$ and $C_t = 87\ pF$, determine the following:

(a) The voltage gain from base to collector
(b) The voltage v_c that will appear at the collector
(b) The overall gain of the amplifier
(b) The value of the output voltage v_o across R_L
(c) The bandwidth of the amplifier

Solution

$$V_B = V_{R_1} = \frac{R_1}{R_1 + R_2} V_{cc} = \frac{3.9k}{3.9k + 18k} \times 15V = 2.671V$$

$$V_E = V_B - V_{BE} = (2.671 - 0.7)V = 1.971V$$

$$I_E = \frac{V_E}{R_E} = \frac{1.971V}{1.2k} = 1.643mA$$

$$r_e = \frac{V_T}{I_E} = \frac{26mV}{1.643mA} = 15.825\Omega$$

$$C_T = C_t + C_S + C_{BC} = (87 + 3.5 + 2.5)pF = 93pF$$

The resonant frequency is given by

$$f_o = \frac{1}{2\pi\sqrt{L_P C_T}} = \frac{1}{2\pi\sqrt{18\mu \times 93p}} = 3.890MHz$$

$$X_L = 2\pi f_o L = 2\pi \times 3.890M \times 18\mu = 439.949\Omega$$

$$R_{coil} = Q_u X_L = 75 \times 439.949\Omega = 32.996k\Omega$$

$$R_L^{'} = \left(\frac{n_p}{n_s}\right)^2 R_L = 10^2 \times 50\Omega = 5k\Omega$$

$$R_c^{'} = R_3 // R^{'}{}_L // R_{coil} = \frac{1}{\frac{1}{R_3} + \frac{1}{R_L^{'}} + \frac{1}{R_{coil}}} = \frac{1}{\frac{1}{5k} + \frac{1}{5k} + \frac{1}{32.996k}} = 2.324k\Omega$$

The gain from the base to the collector is

$$A_v = -\frac{R_c^{'}}{r_e} = -\frac{2.324k\Omega}{15.825\Omega} = -146.856$$

(b) After amplification the input voltage will produce collector voltage v_c, which is inverted

$$v_c = A_v v_{in} = 146.856 \times 50mV = 7.343V$$

(c) The overall gain of the circuit will be

$$A_{vT} = \frac{v_o}{v_{in}} = \frac{\left(\frac{n_s}{n_p}\right)v_c}{v_{in}} = \left(\frac{n_s}{n_p}\right)A_v = \frac{1}{10} \times -146.856 = -14.686$$

In dB, the overall gain is

$$A_{vT}(dB) = 20\log(A_{vT}) = 20\log(14.686) = 23.338dB$$

(d) The output voltage will be

$$v_o = \frac{n_s}{n_p} v_c = \frac{1}{10} \times 7.343V = 734.300V$$

(e) And the bandwidth of the circuit is given by

$$BW = \frac{f_o}{Q_L}$$

where Q_L is the effective or loaded Q of the circuit, which is given by

$$Q_L = \frac{R_c^{'}}{X_L} = \frac{2.324k}{439.949} = 5.282$$

$$\therefore BW = \frac{3.890MHz}{5.282} = 736.463kHz$$

Designing a small signal RF amplifier

To design a small signal RF amplifier the following rules of thumb are used:

1. Set V_E to about 1V or 10% of V_{cc}
2. Current through R_1 to be ten times I_B (i.e. $I_1 \approx 10I_B$)
3. Use maximum efficiency, which is 50%
4. Choose capacitors so that their reactance are in the order of magnitude (10:1) less than the resistance they are used to bypass; that is,
5. V_T = 26 mV
6. R_{dn} =100 **Ω**

From ROT 1: 10% of V_{cc} is used for V_E, then the input dc power will be

$$P_{in} = P_{dc} = 0.9V_{cc}I_c$$

From ROT3: $\%\eta = \frac{P_o}{P_{dc}} \times 100\% = 50\%$

$$\therefore \frac{P_o}{P_{dc}} = \frac{50\%}{100\%} = \frac{1}{2}$$

Substituting $P_{in} = P_{dc} = 0.9V_{cc}I_c$ and re-arranging we get

$$I_c = \frac{2P_0}{0.9V_{cc}} \approx I_E$$

From ROT 6 R_{dn} =100 Ω, and to find the values of other resistors we use Ohm's Law and ROT 1, 2 and 5:

$$r_e = \frac{V_T}{I_E} = \frac{26mV}{I_E}$$

$$R_E = \frac{V_E}{I_E}$$

$$R_1 = \frac{V_B}{I_1} = \frac{V_B}{10I_B}, \text{ where } I_B = \frac{I_C}{\beta}$$

$$R_2 = \frac{V_{cc} - V_B}{1.1I_1} = \frac{V_{cc} - V_B}{11I_B}$$

$$R_{in} = (1+\beta)r_e$$

$$R_{BB} = R_1 // R_2$$

$$R_c^{'} = \frac{r_c}{2} \text{ or}$$

$$R_c^{'} = R_3 // R'_L // R_{coil} \text{ if } r_c \text{ is not given}$$

To find the values of the capacitors, we use ROT 4 as follows:

$$X_{Cdn} = \frac{R_{dn}}{10}$$

$$\therefore C_{dn} = \frac{1}{2\pi f_o X_{Cdn}}$$

$$X_{C_E} = \frac{r_e}{10}$$

$$\therefore C_E = \frac{1}{2\pi f_o X_{C_E}}$$

$$X_{Cc} = \frac{Z_{in}}{10}$$

$$\therefore C_c = \frac{1}{2\pi f_o X_{C_C}}$$

where $Z_{in} = R_{BB} \,//\, R_{in} \,//\, X_{Cin} = \frac{1}{\frac{1}{R_{BB}} + \frac{1}{R_E} + \frac{1}{-JX_{Cin}}}$, and X_{Cin} is given by

$$C_{in} = C_{BE} + \left(1 + |A_V|\right)C_{BC}$$

$$X_{C_T} = X_L = \frac{R_c^{'}}{Q_L}$$

$$\therefore C_T = \frac{1}{2\pi f_o X_{C_T}}$$

The tuning capacitance C_t is

$$C_t = C_T - C_S - C_{BC}$$

And the primary inductance of the transformer is

$$L_S = \frac{X_L}{2\pi f_o}$$

Lastly, the transformer must transform R_L up to match r_c in order to ensure the maximum power transfer. This is done by getting the turns ratio that will be equal to the ratio of r_c to R_L when squared; that is,

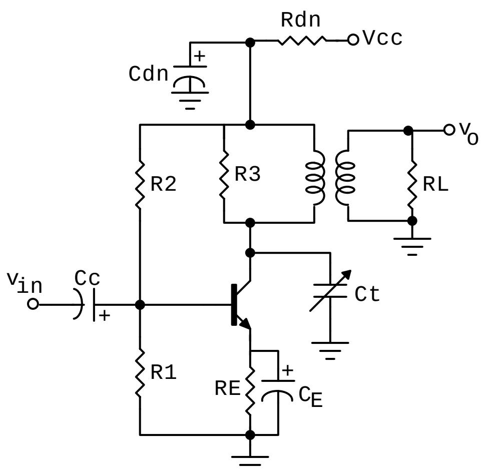
$$\left(\frac{n_p}{n_s}\right)^2 = \frac{r_c}{R_L}$$

$$\therefore\left(\frac{n_p}{n_s}\right)=\sqrt{\frac{r_c}{R_L}}$$

Example 2: Design a small signal RF amplifier that will have a maximum signal power of 10 mW and a maximum power transfer at 98 MHz. Use $V_E = 10\%$ of V_{CC}; $I_1 \approx 10I_B$; $R_{dn} = 100\Omega$; $X_{Cdn} = \frac{R_{dn}}{10}$; $X_{C_E} = \frac{r_e}{10}$; $X_{Cc} = \frac{Z_{in}}{10}$; $V_T = 26\ mV$; $R_L = 50\ \Omega$; $BW = 200\ kHz$; $C_S = 2.5\ pF$; $C_{BE} = 12\ pF$; $C_{BC} = 1.5pF$; $\beta_{dc} = 100$; $V_{cc} = 15\ V$ and collector dynamic impedance of 8 kΩ.

Solution

The circuit of a small signal amplifier is as follows:



Where $$I_c = \frac{2P_0}{0.9V_{cc}} = \frac{2\times 10mW}{0.9\times 15V} = 1.481mA \approx I_E$$

$$I_B = \frac{I_C}{\beta} = \frac{1.481mA}{100} = 14.81\mu A$$

$$V_E = \frac{V_{cc}}{10} = \frac{15V}{10} = 1.5V$$

$$V_B = V_E + V_{BE} = 1.5V + 0.7V = 2.2V$$

The values of the resistor are:

$$r_e = \frac{V_T}{I_E} = \frac{26mV}{1.481mA} = 17.556\Omega$$

$$R_E = \frac{V_E}{I_E} = \frac{2.2V}{1.481mA} = 1.013k\Omega$$

$$R_1 = \frac{V_B}{I_1} = \frac{V_B}{10I_B} = \frac{2.2V}{10 \times 14.81\mu A} = 14.855k\Omega$$

$$R_2 = \frac{V_{cc} - V_B}{1.1I_1} = \frac{V_{cc} - V_B}{11I_B} = \frac{15V - 2.2V}{11 \times 14.81\mu A} = 78.571k\Omega$$

$$R_{in} = (1+\beta)r_e = (1+100)17.556\Omega = 1.773k\Omega$$

$$R_{BB} = R_1 // R_2 = 14.855k // 78.571k = 12.493k\Omega$$

$$R_c^{'} = \frac{r_c}{2} = \frac{8k}{2} = 4k\Omega$$

The gain of the circuit is

$$A_v = \frac{R_c^{'}}{r_e} = \frac{4k}{17.556} = 227.842$$

The values of the capacitors are:

$$X_{Cdn} = \frac{R_{dn}}{10} = \frac{100\Omega}{10} = 10\Omega$$

$$\therefore C_{dn} = \frac{1}{2\pi f_o X_{Cdn}} = \frac{1}{2\pi \times 98 \times 10^6 \times 10} = 162.403\,pF$$

$$X_{C_E} = \frac{r_e}{10} = \frac{17.556\Omega}{10} = 1.756\Omega$$

$$\therefore C_E = \frac{1}{2\pi f_o X_{C_E}} = \frac{1}{2\pi \times 98 \times 10^6 \times 1.756} = 924.846\,pF$$

$$C_{in} = C_{BE} + \left(1 + |A_V|\right)C_{BC} = 12pF + (1 + 227.842)1.5pF = 355.263pF$$

$$Z_{in} = R_{BB} // R_{in} //\left(-jX_{Cin}\right) = \frac{1}{\frac{1}{R_{BB}} + \frac{1}{R_{in}} + \frac{1}{-jX_{Cin}}} = \frac{1}{\frac{1}{12.493k} + \frac{1}{1.773k} + \frac{1}{-j4.571}} = -j4.571\Omega$$

$$X_{Cc} = \frac{Z_{in}}{10} = \frac{4.571\Omega}{10} = 0.457\Omega$$

$$\therefore C_c = \frac{1}{2\pi f_o X_{C_C}} = \frac{1}{2\pi \times 98 \times 10^6 \times 0.457} = 3.553nF$$

$$Q_L = \frac{f_o}{BW} = \frac{98 \times 10^6}{200 \times 10^3} = 490$$

$$X_{C_T} = X_L = \frac{R_c'}{Q_L} = \frac{4k}{490} = 8.163$$

$$\therefore C_T = \frac{1}{2\pi f_o X_{C_T}} = \frac{1}{2\pi \times 98 \times 10^6 \times 8.163} = 198.95pF$$

The tuning capacitance C_t is

$$C_t = C_T - C_S - C_{BC} = 198.95pF - 2.5pF - 1.5pF = 194.95pF$$

And the primary inductance of the transformer is

$$L_S = \frac{X_L}{2\pi f_o} = \frac{8.163}{2\pi \times 98 \times 10^6} = 13.257nH$$

Lastly, the transformer must transform R_L up to match r_c in order to ensure the maximum power transfer. This is done by getting the turns ratio that will be equal to the ratio of r_c to R_L when squared; that is,

$$\therefore \left(\frac{n_p}{n_s}\right) = \sqrt{\frac{r_c}{R_L}} = \sqrt{\frac{8k}{50}} = 12.65:1$$

Neutralization

When the amplifying device is operated near its upper-cutoff frequency, a parasitic capacitance C_f is developed between its input and output as shown in Figure 2.

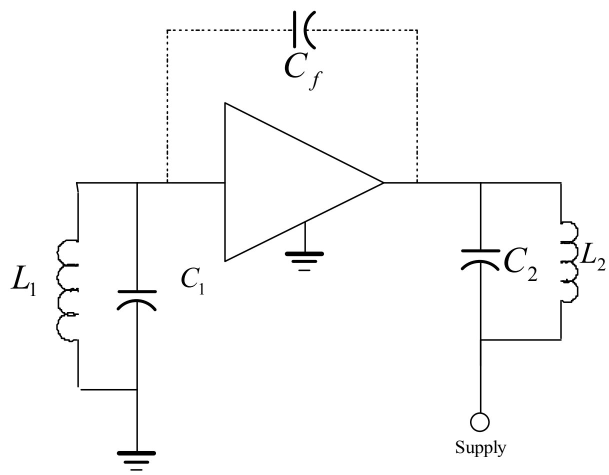


Figure 2 RF amplifier with a parasitic feedback capacitance C_f

This C_f provides path for feedback, which can cause the circuit to be unstable and tend to oscillate. In order to cancel the effects of the parasitic feedback capacitance and provide stability to the amplifier *neutralization* is used. There are several schemes of neutralization, but here the discussion will be limited to two: *Hazeltine* and *Rice* neutralization systems.

Hazeltine Neutralization System

Figure 3 shows a Hazeltine neutralizing system where the output coil L_2 is center-tapped, and the tap is used as the feedpoint for the power supply to amplifier. The bottom end of the output coil is connected through a small capacitor, called *neutralizing capacitance* C_N back to the input of the amplifier.

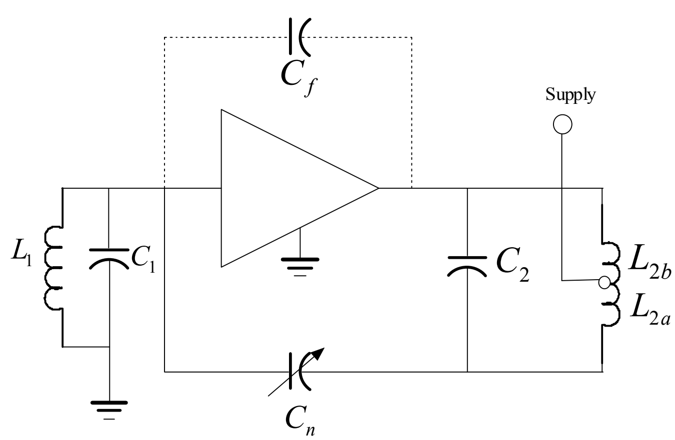


Figure 3 Hazeltine neutralization system.

The portion of the circuit formed by the amplifier output voltage, the two halves of the output coil (L_2), the feedback capacitance (C_f) and neutralizing capacitance (C_n) form a bridge to the input of the amplifier.
For the bridge to null, producing a zero voltage across the amplifier input, the impedance cross products must be equal; that is,

$$X_{Cf} X_{L2a} = X_{Cn} X_{L2b}$$

And

$$C_n = C_f \frac{L_{2b}}{L_{2a}} = C_f \text{ (since } L_2 \text{ is center-tapped)}$$

Rice Neutralization

The circuit for the Rice method of neutralization is as shown in Figure 4 below:

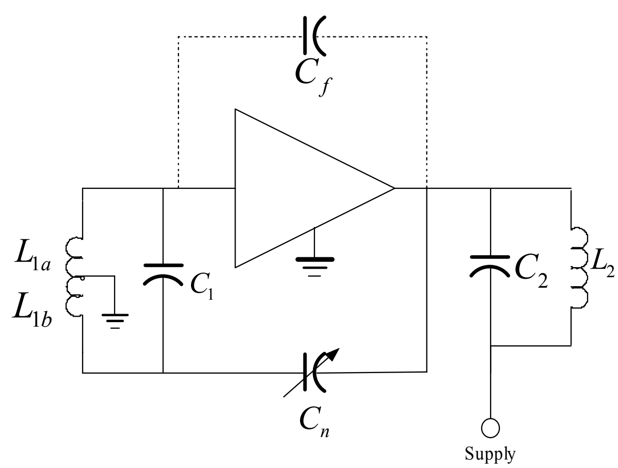


Figure 4 Rice neutralization system

The input coil L_1 is center-tapped so that $L_{1a} = L_{1b}$. A neutralization capacitance C_n, which is equal to the parasitic feedback capacitance, is connected between the bottom-end of input coil L_1 and the output of the amplifier. The voltage appearing at the output of the amplifier drives a phase-shifted current through C_f and L_{1a}, producing a voltage at the amplifier input. However, the same output voltage also drives an identical-valued current in the opposite direction through C_n and L_{1b}. Therefore the currents in L_1 will be equal and opposing, thereby resulting in a zero feedback voltage appearing at the input of the amplifier. This null will only occur when

$$XC_f = XC_n$$

so that $$C_f = Cn$$

MIXERS

Mixers are circuits that are used in both high frequency radio transmitters and receivers for performing *heterodyning* or *frequency conversion*; that is, changing of the carrier frequency with its modulation from one frequency to another frequency that is either higher or lower. In transmitters mixers are used to convert the carrier frequency and its modulation to a higher frequency; that is, they up–convert. In receivers, mixer stage is placed immediately after the RF stage to convert the selected frequency from RF to another frequency, which is usually lower; that is they down-convert. The mixer takes the selected signal from the RF stage, v_s, at frequency f_s and mixes it with the signal that is generated by the local oscillator, v_o, at frequency f_o to produce a new set of frequencies, which include, among its components, the two frequencies (f_o and f_s), their sum ($f_o + f_s$), and their difference ($f_o - fs$). At the output of the mixer there is another tuned circuit that couples the mixer stage to the IF stage. This tuned circuit has a bandpass response to only pass one frequency component together with its modulation and attenuate all other frequency components.

The output of the mixer is referred to as the *IF signal* and is usually current i_{IF}, which has a magnitude that is proportional to the amplitude of the selected signal, V_s. The proportionality constant is given by

$$g_c = \frac{|i_{IF}|}{V_s}$$

and is called *conversion transconductance*, g_c. At the heart of each mixer circuit there is a nonlinear device such as diode, BJT or FET, which has square law characteristics. Mixers can also be built using integrated circuits. Mixers that are designed using BJT, FETs and ICs are sometimes referred to as active mixers while those that are designed using diodes only are referred to as passive mixers. Active mixers are the most commonly used than the passive ones because they provide an additional gain in addition to frequency conversion. According to Young (p.220) the output versus input nonlinearity of any device can be expressed mathematically by a power series such as

$$i_o = I_o + av_i + bv_i^2 + cv_i^3 + ...nv_i^n$$

There are two basic methods used for mixing: additive and multiplicative mixing. The difference between the two depends on how the RF signal and the local oscillator signal are applied to the nonlinear device. Some mixer circuits are shown below.

Additive mixing

In additive mixing the selected signal from the RF stage, v_s, is simple added to the output of the local oscillator, v_o. The magnitude of V_o is made to be much larger than V_s so that a large transconductance can be obtained. Their sum v_i is passed through a nonlinear device that has square law characteristics as shown in the Figure 1.

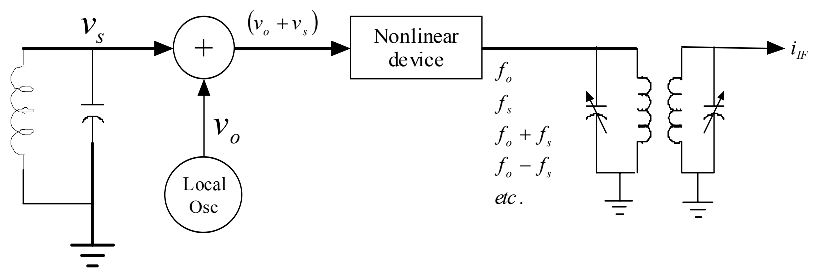


Figure 1 Additive Mixer

The output of the nonlinear device contains among its components the two frequencies, their sum, their difference, and other frequencies that are harmonics of the input frequencies. The output is passed through a tuned circuit, which couples the mixer to the IF stage that has a bandpass response so that only the difference of the two frequencies can be passed to the IF stage. Mathematically, the additive mixing can be analyzed as follows:

The sum is: $v_i = v_o + v_s$

If a diode or a FET is used as a nonlinear device, the output current will be in the form

$$\begin{aligned} i_o &= I_d + av_i + bv_i^2 + \ldots \\ &= I_d + a(v_o + v_s) + b(v_o + v_s)^2 + \ldots \\ &= I_d + av_o + av_s + b(v_o^2 + 2v_o v_s + v_s^2) + \ldots \\ &= I_d + av_o + av_s + bv_o^2 + 2bv_o v_s + bv_s^2 + \ldots \end{aligned}$$

Substituting $V_s sin w_s t$ for v_s and $V_o sin w_o t$ for v_o we get

$$i_o = I_d + aV_s \sin w_s t + aV_o \sin w_o t + bV_o^2 \sin^2 w_o t + 2bV_o V_s \sin w_o t \sin w_s t + bV_s^2 \sin^2 w_s t + \ldots$$

Using trigonometric identities to expand $\sin w_o t \sin w_s t$ we get

$$\begin{aligned} i_o = I_d + aV_s \sin w_s t + aV_o \sin w_o t + bV_o^2 \sin^2 w_o t + bV_o V_s [\cos(w_o - w_s)t - \cos(w_o + w_s)t] \\ + bV_s^2 \sin^2 w_s t + \ldots \end{aligned}$$

$$\begin{aligned} = I_d + aV_s \sin w_s t + aV_o \sin w_o t + bV_o^2 \sin^2 w_o t + bV_o V_s \cos(w_o - w_s)t - bV_o V_s \cos(w_o + w_s)t \\ + bV_s^2 \sin^2 w_s t + \ldots \end{aligned}$$

This current is passed through a tuned circuit that is connected to the output of the mixer. After the bandpass filtering by the output tuned circuit, the final output current is

$$i_{IF} = bV_o V_s \cos(w_o - w_s)t$$

if we are down-converting, or

$$i_{IF} = bV_o V_s \cos(w_o + w_s)t$$

if we are up-converting, and all the other frequency components are attenuated.

Multiplicative Mixing

In multiplicative mixing both the output of the RF and that of the local oscillator are fed directly to the multiplying device as shown in Figure 2 below.

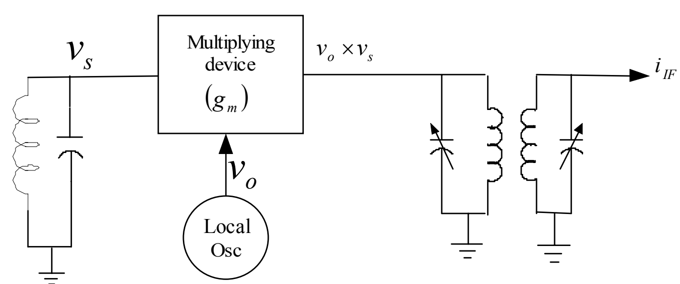


Figure 2 Multiplicative mixer

The transconductance, g_m, of the multiplying device is caused to vary with output of the local oscillator, thus resulting in an output current which is a function of the product of the two input signals, v_s and v_o. Mathematically, the multiplicative mixing can be analyzed as follows:

The output current of the multiplying device is

$$i_m = g_m v_s$$

where the transconductance g_m is a function of oscillator voltage. The value of g_m may be stated in terms of the Fourier series as

$$g_m = a_o + a_1 \cos w_o t + \ldots$$

Substituting for g_m in the output current i_m yields

$$
\begin{aligned}
i_m &= (a_o + a_1 \cos w_o t + \ldots) v_s \\
&= (a_o + a_1 \cos w_o t + \ldots) V_s \cos w_s t \\
&= a_o V_s \cos w_s t + a_1 V_s \cos w_o t \cos w_s t + \ldots
\end{aligned}
$$

Using trigonometric identities to expand $\cos w_o t \cos w_s t$, we get

$$
\begin{aligned}
i_m &= a_o V_s \cos w_s t + \frac{a_1 V_s}{2} [\cos(w_o - w_s)t + \cos(w_o + w_s)t] + \ldots \\
&= a_o V_s \cos w_s t + \frac{a_1 V_s}{2} \cos(w_o - w_s)t + \frac{a_1 V_s}{2} \cos(w_o + w_s)t + \ldots
\end{aligned}
$$

This current is passed through a tuned circuit that is connected to the output of the mixer. This tuned circuit has a band pass response that will only allow the difference of the two frequencies to pass; that is, the output of the tuned circuit will be

$$
i_{IF} = \frac{a_1 V_s}{2} \cos(w_o - w_s)t
$$

if we are down-converting, or

$$
i_{IF} = \frac{a_1 V_s}{2} \cos(w_o + w_s)t
$$

if we are up-converting, and all the other frequency components are attenuated.

TRACKING

In superheterodyne radio receivers the RF stage is gang-tuned together with the local oscillator so that the local oscillator can generate a signal v_o that is precisely IF greater than the selected frequency signal v_s all the time. However, since the circuits of the RF stage and the oscillator are performing different functions, they cannot be the same, thus making it very difficult to maintain the IF difference between them.

To mitigate the possibility of having IF that varies over the tuning range, an additional capacitance and a different value of inductance is used in the local oscillator stage to adjust the capacitance of the local oscillator in order to raise the generated frequency to a value that is IF above the RF signal. These extra capacitors are called *trimmers* and *padders*. A padder capacitor C_p is usually connected in series with the tuning capacitor, whereas the trimmer capacitor C_T is usually placed in parallel with the tuning capacitor. For tracking either one or both of the capacitors are used. Padder adjustment allows the oscillator to match the required frequency at either end of the range, while creating a positive tracking error at midband. Trimmer adjustment allows the oscillator to match the required frequency at either end of the range, while creating a negative tracking error at midband. Combination of trimmer and padder can be used to minimize the tracking error by giving a zero tracking error at both ends of the range and midband. Figure 3 shows these three tracking methods.

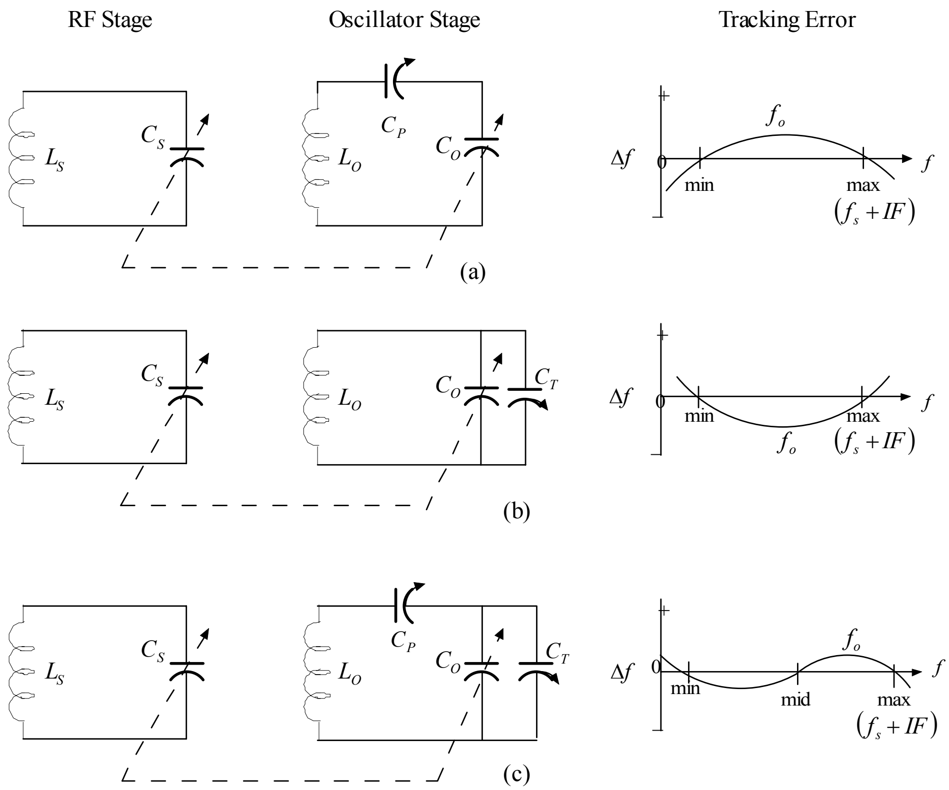


Figure 3 Tracking methods: (a) Padder tracking; (b) Trimmer tracking; (c) Three-point tracking

The value of the padder and the trimmer capacitors is derived from the following equations:

Using a padder:

$$C_o = C_s ser.C_p = \frac{C_s C_p}{C_s + C_p}$$

$$\frac{C_{o_{max}}}{C_{o_{min}}} = \frac{C_{s_{max}} ser.C_p}{C_{s_{min}} ser.C_p} = \frac{C_{s_{max}}(C_{s_{min}} + C_p)}{C_{s_{min}}(C_{s_{max}} + C_p)} = C_{s_{ratio}}\left[\frac{C_{s_{min}} + C_p}{C_{s_{max}} + C_p}\right]$$

At midpoint

$$\frac{C_{s_{\max}}}{C_{s_{mid}}} = \left(\frac{f_{s\,mid}}{f_{s_{\min}}}\right)^2 = C_{s_{mid(ratio)}}$$

Therefore

$$C_{s_{mid}} = \frac{C_{s_{mid}}}{C_{s_{mid(ratio)}}}$$

And

$$C_{o_{mid}} = C_{s_{mid}} ser.C_p = \frac{C_{s_{mid}} \times C_p}{C_{s_{mid}} + C_p}$$

The actual value of the oscillator frequency is given by

$$f_{o_{mid(actual)}} = \frac{1}{2\pi\sqrt{L_o C_{o_{mid}}}}$$

While the desired value is

$$f_{o_{mid(desired)}} = f_{s_{mid}} + IF$$

Therefore, the tracking error is the difference between the actual and the desired value; that is,

$$err = f_{o_{mid(actual)}} - f_{o_{mid(desired)}}$$

Using a trimmer:

$$C_o = C_s par.C_T = C_s + C_T$$

$$\frac{C_{o_{max}}}{C_{o_{min}}} = \frac{C_{s_{max}} par.C_T}{C_{s_{min}} par.C_T} = \frac{C_{s_{max}} + C_T}{C_{s_{min}} + C_T}$$

The oscillator coil is given by

$$L_o = \frac{1}{\left(\omega_{o_{min}}\right)^2 C_{o_{max}}} = \frac{1}{\left(\omega_{o_{max}}\right)^2 C_{o_{min}}}$$

Example 1: An AM superheterodyne receiver is designed to receive over a range of frequencies from 550 to 1650 kHz. If IF is 465 kHz and Cs_{max} = 390 pF, find the value of padder capacitor and oscillator inductor required to give two-point tracking. Also determine the error in oscillator tracking frequency for a signal at a frequency that is midway between the lower and the higher values of the tuning range.

Solution

Given $f_s = (550 \rightarrow 1650)kHz$ and $IF = 465kHz$

$$\therefore f_o = [(550 \rightarrow 1650)465]kHz = (1015 \rightarrow 2115)kHz$$

$$\frac{C_{s_{\max}}}{C_{s_{\min}}} = \left(\frac{f_{s_{\max}}}{f_{s_{\min}}}\right)^2 = \left(\frac{1650k}{550k}\right)^2 = 9$$

If $C_{s_{\max}} = 390pF$, then $C_{s_{\min}}$ will be

$$C_{s_{\min}} = \frac{C_{s_{\max}}}{9} = \frac{390pF}{9} = 43.333pF$$

$$\frac{C_{o_{\max}}}{C_{o_{\min}}} = \left(\frac{f_{o_{\max}}}{f_{o_{\min}}}\right)^2 = \left(\frac{2115k}{1015k}\right)^2 = 4.342$$

$$\frac{C_{o_{max}}}{C_{o_{min}}} = \frac{C_{s_{max}} ser.C_p}{C_{s_{min}} ser.C_p} = \frac{C_{s_{max}}(C_{s_{min}} + C_p)}{C_{s_{min}}(C_{s_{max}} + C_p)} = C_{s_{ratio}}\left[\frac{C_{s_{min}} + C_p}{C_{s_{max}} + C_p}\right]$$

$$\therefore \qquad 9\left[\frac{43.33p + C_p}{390p + C_p}\right] = 4.342$$

$$43.333p + C_p = 188.153p + 0.482C_p$$

$$\therefore \qquad 0.518C_p = 144.820$$

$$C_p = 279.575pF$$

Using $C_o = C_s ser.C_p = \dfrac{C_s C_p}{C_s + C_p}$ we get

$$C_{o_{\max}} = \frac{390\text{p} \times 279.575\text{p}}{390\text{p} + 279.575\text{p}} = 162.841\text{pF}$$

And

$$C_{o_{\min}} = \frac{43.333\text{p} \times 279.575\text{p}}{43.333\text{p} + 279.575\text{p}} = 37.518\text{pF}$$

The oscillator coil is given by

$$L_o = \frac{1}{\left(\omega_{o_{\min}}\right)^2 C_{o_{\max}}} = \frac{1}{\left(\omega_{o_{\max}}\right)^2 C_{o_{\min}}} = \frac{1}{\left(2\pi \times 2115k\right)^2 \times 37.518p} 150.931\mu H$$

At midpoint

$$\frac{C_{s_{\max}}}{C_{s_{mid}}} = \left(\frac{f_{s\,mid}}{f_{s_{\min}}}\right)^2 = C_{s_{mid(ratio)}} = \left(\frac{1100k}{550k}\right)^2 = 4$$

Therefore

$$C_{s_{mid}} = \frac{C_{s_{mid}}}{C_{s_{mid(ratio)}}} = \frac{390p}{4} = 97.5pF$$

And

$$C_{o_{mid}} = C_{s_{mid}} ser.C_p = \frac{C_{s_{mid}} \times C_p}{C_{s_{mid}} + C_p} = \frac{97.5p \times 279.575p}{97.5p + 279.575p} = 72.289pF$$

The actual value of the oscillator frequency is given by

$$f_{o_{mid(actual)}} = \frac{1}{2\pi\sqrt{L_o C_{o_{mid}}}} = \frac{1}{2\pi\sqrt{150.931\mu \times 72.289p}} = 1516kHz$$

While the desired value is

$$f_{o_{mid(desired)}} = f_{s_{mid}} + IF = (1100 + 465)kHz = 1565kHz$$

Therefore, the tracking error is the difference between the actual and the desired value; that is,

$$err = f_{o_{mid(actual)}} - f_{o_{mid(desired)}} = 1516kHz - 1565kHz = -49kHz$$

IF STAGE

IF stage comes immediately after the mixer stage and is responsible for the provision of the bulk of the gain of the radio receiver. On average the IF stage must provide a gain of 60 to 80 dB so that the level of the signal fed to the detector is high enough for the detector to perform adequately. Additional to provision of the gain, the IF stage is also responsible for the following:

- Providing a fixed bandpass filtering throughout the entire frequency range of the receiver as opposed to the varying bandpass bandwidth that is provided by the RF stage, which means that the superheterodyne has RF stage and a fixed bandpass IF stage for determining the selectivity of the receiver. This helps to keep the overall bandwidth of the receiver constant, thus making the superheterodyne receiver to have better selectivity than TRF receiver that relies only on RF stage for selectivity.
- Providing automatic gain control (AGC) for maintaining a relative constant signal output even if the strength of the received signal is varying. AGC is usually provided in the first stage of the IF amplifier.
- In the case of FM receivers, the IF stage must also provide signal amplitude limiting that is required in FM reception in order to make sure that the IF signal presented to the FM detector or discriminator has only frequency variations and no amplitude variations. Amplitude limiting is usually provided in the last stage of the IF amplifier.

The IF stage consists of two or more cascaded amplifier stages that are operating around IF, and since they are operating at a fixed frequency, double-tuned circuits are used to couple different IF amplifier stages, thus allowing for sharply defined bandpass response. The bandwidth of the bandpass of these tuned circuits depends on the type of the signal it is to handle. For example, for AM broadcast receivers, the ideal bandwidth must be about 10 kHz; for narrow-band voice communication FM receivers the bandwidth is about 30 kHz; for FM broadcast receivers the bandwidth is 200 kHz, and for TV the bandwidth is in the order of 6 to 12 MHz. In order to obtain the required bandpass filter response from the IF stage, a technique called *stagger tuning* is used.

Stagger tuning

Stagger tuning involves the alignment of successive tuned circuits to slightly different frequencies in order to widen the overall amplitude-frequency response curve. This is done by means of under-critically coupling the coupling transformers to prevent the occurrence of double humps on their responses. This makes each tuned circuit to be effectively isolated from all the others and to act independently to provide its own response (resonance curve). The individual responses are finally added to produce the overall response of the IF stage as shown in Figure 1. The Q’s are chosen so that the overall response has a 3-dB bandwidth of the required bandpass and steeper roll-offs.

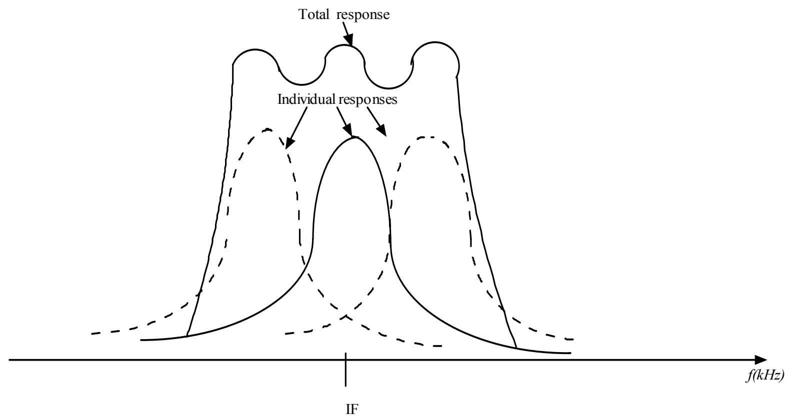


Figure 1 Stagger tuning response curves

Automatic gain Control

The automatic gain control (AGC) circuit is responsible for compensating for the variations in the received signal levels. This is done by varying automatically the gain of the receiver with the changing strength of the received signal in order to keep the output substantially constant. AGC is accomplished by sensing the output of the demodulator stage and generating a dc voltage called *AGC bias* that is used to adjust the gain of IF stage, or IF and RF stages. The former is referred to as the *simple AGC* and it only involves the adjustment of the gain of the IF amplifiers while the latter is called *delayed AGC* and it involves the application of AGC bias to both IF and RF amplifiers; however, the AGC applied to the RF stage is delayed until a suitable signal-to-noise ratio is reached hence it is referred to as delayed AGC. The range of levels; that is, the minimum to maximum signal strength over which the receiver will be able to keep the output constant is called the *system dynamic range*.

Simple AGC is used for most of the domestic receivers and cheaper communication receivers. In simple AGC, the AGC bias starts to increase as soon as the received signal exceeds the background noise thereby decreasing the gain of the receiver, and making the receiver less sensitive. Delayed AGC, on the other hand, is used for better broadcast and communication receivers. Here the AGC bias for the RF stage is delayed until a signal exceeds a preset threshold voltage. This is done to allow the RF stage to perform other functions such as improving the signal-to-noise ratio before AGC. This enables the signals below the set threshold to be passed through with maximum gain thereby improving the signal-to-noise ratio of the receiver even when weak signals are received. Another advantage of using delayed AGC is that when a strong signal is received, delayed AGC will be able to control the gain of the RF stage so that the signal does not overload the RF and the mixer stage, whereas if only simple AGC was used the strong signal will overload both RF and mixer stage thereby resulting in a distorted signal being fed to the IF stage. Figure 2 shows the response of a receiver with simple and delayed AGC compared to one with no AGC.

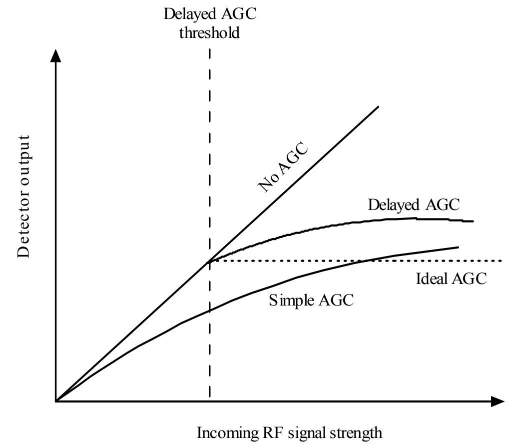


Figure 2 AGC characteristics

Most of the AGC systems work by taking the output of the demodulator or detector stage average it to produce a dc voltage called AGC bias voltage, which is proportional to the level of the received signal. The resultant AGC voltage is used to vary the biasing, hence the gain, of the IF or RF amplifier. To convert the demodulator output to an AGC signal a simple low pass filter is normally used. This low pass filter consists of a simple resistor capacitor (RC) network with a time constant that is at least 10 times longer than the period of the lowest modulating frequency. Figure 3 shows a typical AGC system where the output of the detector is averaged by a RC low pass filter formed by resistor R_g and capacitor C_g. The AGC bias produced by the RC network is fed to the input of the amplifier to vary its bias voltage and consequently its gain. The polarity of the AGC voltage is chosen such that an increase in the received signal will produce an increase in the magnitude of the AGC bias voltage which will result in a decrease in the bias voltage and a reduction in the gain of the amplifier. For example, in Figure 3 the orientation of diode D_1 is such that the polarity of the AGC voltage is negative; that is, opposite to that of the bias voltage so that as it increases it subtracts from bias voltage thereby reducing it and the gain of the amplifier. Conversely, a decrease in the received signal will result in a decrease in the magnitude of the produced AGC voltage thereby resulting in an increase in the bias voltage in the gain of the amplifier. Figure 3 also shows how to generate a delayed AGC. Diode D_2 together with resistors R_1, R_2 and R_3 set the threshold value that must be overcome before the AGC bias is passed on to control the RF amplifier gain. Resistors R_1, R_2 and R_3 place a positive bias voltage at anode of diode D_2 to keep it reversed until the AGC bias rises up to the threshold value. R_3 can be used to adjust the threshold value.

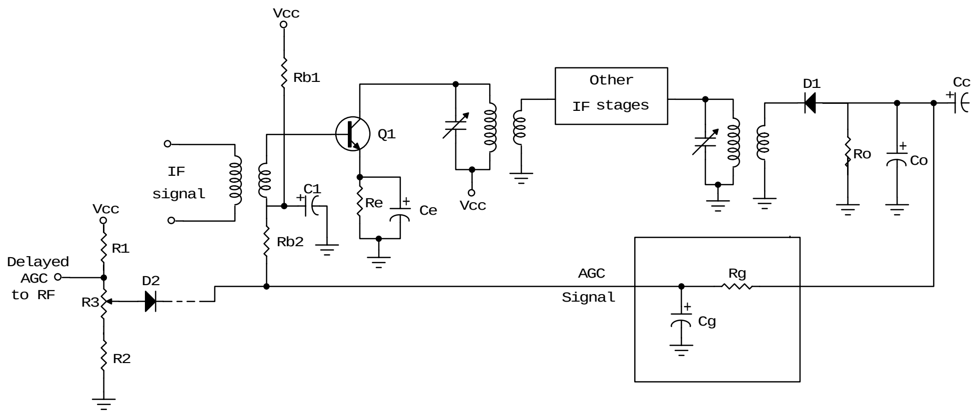


Figure 3 AGC System

Amplitude limiting

FM receivers have another stage called a limiter. Though in FM block diagrams the limiter is shown as a stand-alone stage between the IF and detector, in practical receiver circuits the limiter is integrated within the IF stage. One of the IF amplifiers, usually the last one, is designed such that it provides the maximum gain until the output signal level reaches a predetermined threshold, then for any input signal above this the output remains constant at a threshold. This guarantees that the level of the signal presented to the detector stage has constant amplitude in order to prevent output distortions that come as a result of amplitude variations in the IF signal.

Automatic Frequency control

Automatic frequency control (AFC) system is used in both radio transmitters and radio receivers to make sure that the transmitter or the receiver stays on the correct frequency; that is, it ensures the frequency stability of the transmitter or receiver.

In transmitters AFC is used to correct carrier drift and in receivers the AFC circuit is used to provide a slight automatic control over the local oscillator circuit to compensate for the drift in the local oscillator frequency that would otherwise cause a station to be detuned. However, new methods have been found on how to provide sufficient frequency stability without the use of AFC as a result most of new designs exclude AFC circuits.

DEMODULATION

After the signal has been amplified by the IF stage it is fed to the detector where the original modulating signal, information or intelligence is extracted or recovered from the incoming modulated signal. This process, which is the reverse of the modulation by which the modulating signal is superimposed into the station carrier during transmission, is called *demodulation*. Since the circuits for generating AM are different from that of FM, even when it comes to demodulation, the AM detectors are completely different from FM detectors.

AM DEMODULATORS

There are two most commonly used AM detectors: Envelope detector and product detector. Envelope detector is used for double sideband full carrier (DSBFC) and vestigial sideband (VSB) signals while the product detector is used for double sideband suppressed carrier (DSBSC) and single sideband suppressed carrier (SSBSC) signals. The prerequisite for using an envelope detector is the presence of a strong carrier and a high signal-to-noise ratio, while the prerequisite for using a product detector is the reinsertion of a carrier that has exactly the same frequency and phase as the original suppressed carrier. Demodulation using an envelope detector is non-coherent, while the one using a product detector is coherent. Non-coherent envelope detector is very simple while the coherent product detector is complex because of its associated carrier recovery circuitry. However, noise performance of a coherent detector is always better than that of its non-coherent counterpart.

Envelope detector

The envelope detector, which is also known as peak or diode detector, consists of a germanium diode in series with a parallel resistor-capacitor network as shown in Figure 1.

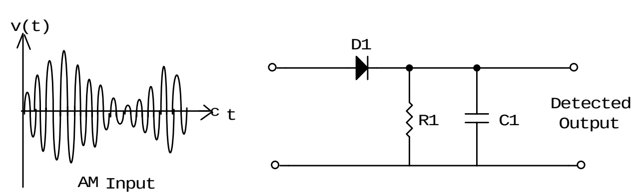


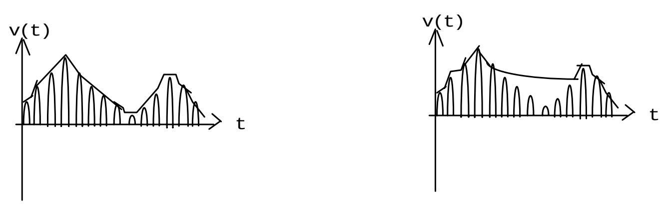
Figure 1 Envelope detector

The diode D_1 will only conduct during the positive half-cycles thereby eliminating all the negative half-cycles. The resultant output will be just the positive peaks of the input modulated carrier. The average value of the resultant output will rise and fall at the same rate as the modulating signal. During the positive half-cycle capacitor C_1 charges to the positive peak voltage through the small resistance of the conducting diode. During the negative half-cycle the capacitor will discharge slowly through resistor R_1 and when the next positive peak arrives the capacitor will start charging again. This process of changing and discharging will continue resulting in a detected output which is a varying voltage that follows the peak variation of the modulated carrier and since the peak variations of the modulated carrier are following the shape of the modulating signal, the detected output will be the same in shape as the original modulating signal.

The values of resistor R_1 and capacitor C_1 must be chosen such that they offer a short time constant at audio frequencies (AF) and a very long time constant at radio frequencies (RF). This is necessary for obtaining optimum efficiency of the envelope detector. If the value of C_1 is too large, R_1C_1 time constant will be too long at AF. This will cause the capacitor not to be able to discharge fast enough for the output to follow the variations of the envelope of the modulated carrier, another problem will be that several cycles will be required to charge up C_1 and this will also result in an output which does not follow the envelope of the modulated carrier. This phenomenon is called *diagonal clipping* because of the diagonal appearance of the discharge curve. Its effect can result in a considerable loss of information. The optimum value or the *RC* constant that will guarantee that there is no diagonal clipping is given by

$$\tau = R_1 C_1 \leq \frac{1}{w_{m(max)}}\sqrt{\frac{1}{m_a^2} - 1}$$

Figure 2 below shows the two detector outputs: one with the correct *RC* constant and the other with a *RC* constant that is too large; that is, the one with diagonal clipping.



(a) Correct *RC* **(b) *RC* too large**

Figure 2 Detector outputs: (a) Correct RC and (b) Diagonal clipping due to large RC

As it can be seen from Figure 2a, the output of the envelope detector has a dc component, which is usually removed using a capacitor to couple the detector to the audio amplifier stage.

Product detector

Unlike DSBFC, the envelope of a DSBSC and SSBSC does not follow the modulating signal hence the received modulated signal cannot be demodulated by an envelope detector. In order to demodulate these signals a special detector called *product detector* is used. For the product detector to work the carrier that was suppressed at the transmitter must be regenerated and reinserted. The locally regenerated carrier must be coherent or synchronized; that is, it must have exactly the same frequency and phase as the original suppressed carrier. If not, there will be severe distortion in the demodulated signal that can result in its phase being altered.

In order to ensure synchronization between the original carrier and the re-inserted carrier, a pilot carrier is usually transmitted together with the suppressed carrier signal to the receiver. In the receiver the pilot signal is used as a reference to generate the coherent carrier; that is, it synchronize the local beat frequency oscillator (BFO) to produce a carrier that has exactly the same frequency and phase as the original suppressed carrier. At the heart of the product detector is an analog multiplier (nonlinear mixer or a balanced modulator), which is used to nonlinearly mix the incoming suppressed carrier signal *m(t)* (which can either be DSBSC or SSBSC) with the coherent carrier to produce an output that is the product of the two signals, v_m; that is, it multiplies the incoming modulated signal with the coherent carrier. Mathematically, the analysis of the product detector is as follows:

$$v_m = m(t).v_c$$

Assuming the incoming suppressed carrier signal *m(t)* to be a DSBSC, then v_m will be

$$\begin{aligned}
v_m &= v_{DSBSC} \times v_c \\
&= [cos(w_c - w_m)t - cos(w_c + w_m)t]sin\, w_c t \\
&= cos(w_c - w_m)t\, sin\, w_c t - cos(w_c + w_m)t\, sin\, w_c t \\
&= \frac{1}{2}[sin(w_c - w_m + w_c)t - sin(w_c - w_m - w_c)t] \\
&\quad - \frac{1}{2}[sin(w_c + w_m + w_c)t - sin(w_c + w_m - w_c)t] \\
&= \frac{1}{2}[sin(2w_c - w_m)t - sin(-w_m)t] - \frac{1}{2}[sin(2w_c + w_m)t - sin(w_m)t] \\
&= \frac{1}{2}sin(2w_c - w_m)t + \frac{1}{2}sin\, w_m t - \frac{1}{2}sin(2w_c + w_m)t + \frac{1}{2}sin\, w_m t \\
&= \frac{1}{2}sin(2w_c - w_m)t - \frac{1}{2}sin(2w_c + w_m)t + sin\, w_m t
\end{aligned}$$

The output of the multiplying device is fed into a low pass filter that will only allow the audio frequency component $sin(w_m)t$ to pass through while attenuating all the other frequency components. Demodulation by means of using a product detector is known as coherent detection or synchronous demodulation and is not only limited to the demodulation of suppressed carrier signal but can be used to modulate almost any AM signal. Figure 3 shows the block diagram of a product detector and Figure 4 shows a circuit of a product detector using an IC balanced modulator, LM1496/1596.

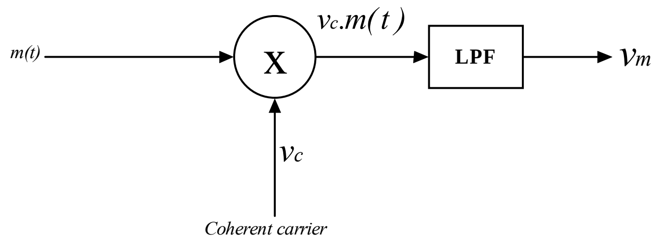


Figure 3 Product detector

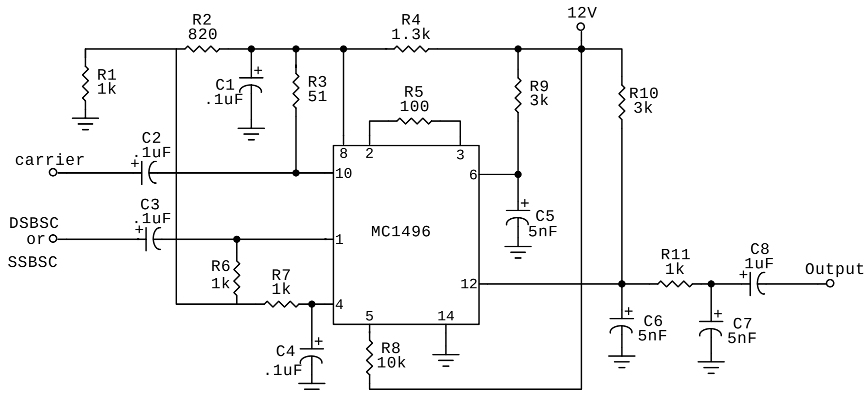


Figure 4 Product detector using MC1496 with a 12Vdc single supply

FM DEMODULATORS

During transmission, FM systems have their carrier frequency varied in accordance with the modulating signal. Therefore in order to recover the original modulating signal from the incoming FM signal, the receiver must be able to convert frequency variations into voltage whose magnitude is proportional to the frequency deviation of the incoming FM signal. This phenomenon is called *frequency demodulation* or *discrimination* and there are various techniques and circuits that can be used to accomplish this, which include slope detector, Foster-Seeley detector, ratio detector, quadrature detector, and phase lock loop. Slope detectors are rarely used due to their poor linearity; Foster-Seeley and ratio detector are classical means of demodulating FM that use discrete components and were used mostly with receivers that are using discrete components; quadrature detectors and phase lock loop are the mostly commonly used with today's IC radio receivers.

Slope detector

The slope detector is a basic FM detector, which first converts the frequency variations of the incoming FM signal into amplitude variations and thereafter uses an envelope detector to recover the modulating signal from the amplitude variations. Figure 5 shows a circuit of a lope detector together with the magnitude of its output voltage plotted against the incoming FM signal.

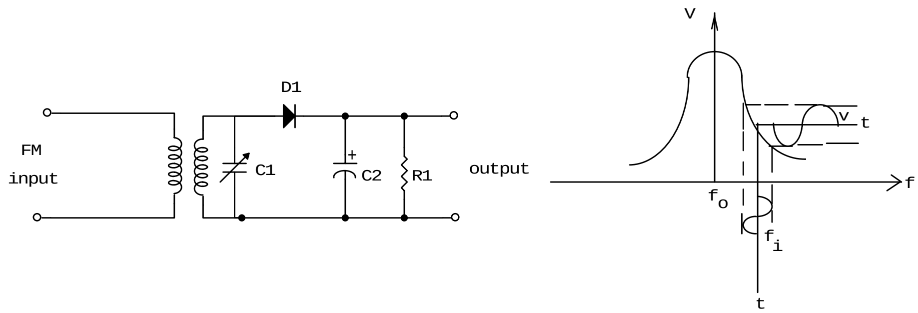


Figure 5 Slope detector circuit and output voltage plotted against frequency

To change the frequency variations to amplitude variations, the tuned circuit that couples the IF/limiter to the detector is detuned such that the carrier frequency f_c lies on either the ascending or descending slope of the response curve. For the discussion here the descending slope has been used as shown in Figure 5. As the incoming signal frequency f_i increases above f_c the voltage across the secondary of the tuned circuit will drop. Conversely, when the incoming signal frequency f_i decreases below f_c the voltage across the secondary of the tuned circuit will rise. This change in voltage due to frequency changes is because of the changes in the magnitude of the tuned circuit's impedance as a function of frequency. The voltage variations are fed to an envelope detector, which is formed by diode D_1, capacitor C_2 and resistor R_1. The envelope detector recovers the modulating signal from the amplitude variations that are produced by the tuned circuit.

One of the disadvantages of the slope detector is poor linear response, which is due to the limited linear range on the voltage/frequency transfer characteristics of the tuned circuit used to convert frequency variations into amplitude variations. This can be improved by using a *balanced slope detector*, also known as *Round-Travis detector*, which combines two slope detector circuits in a balanced configuration as shown in Figure 6. One slope detector is tuned to lie on the ascending slope at f_{o2} while the other is tuned to lie on the descending slope of the response curve at f_{o1}. When the input carrier is unmodulated, the output is balanced to zero. When the carrier deviates towards f_{o2}, the magnitude of the voltage across the bottom half of the secondary V_{o2} will decrease while the voltage across the top half of the secondary V_{o1} will increase; when the carrier deviates towards f_{o1}, the magnitude of the voltage across the bottom half of the secondary V_{o2} will increase while the voltage across the top half of the secondary V_{o1} will decrease. The resulting amplitude variations are fed to the corresponding envelope detectors to produce voltages V_{o1} and V_{o2}, respectively. The outputs of the envelope detectors are combined to give a differential output V_o, which is negative when deviation is towards f_{o2} and positive when deviation is towards f_{o1}.

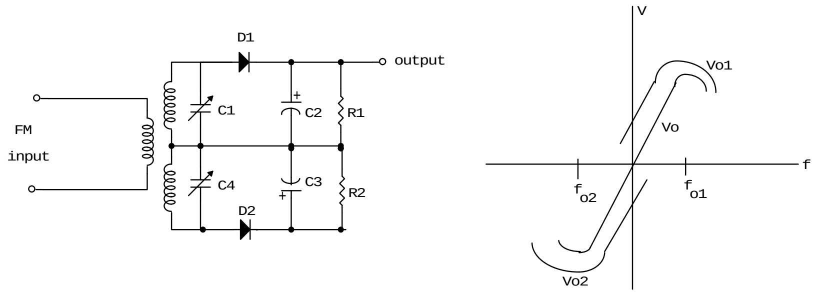


Figure 6 Balanced slope detector circuit and output voltage plotted against frequency

Quadrature detector

A basic quadrature detector consists of phase detector with a has a high-reactance capacitor connected across its input, an LC-tuned circuit and a low pass filter as shown in Figure 7. The tuned circuit is resonant at the carrier frequency. Quadrature detectors are generally available as integrated circuits, either as standalone or within a radio receiver IC that includes other stages.

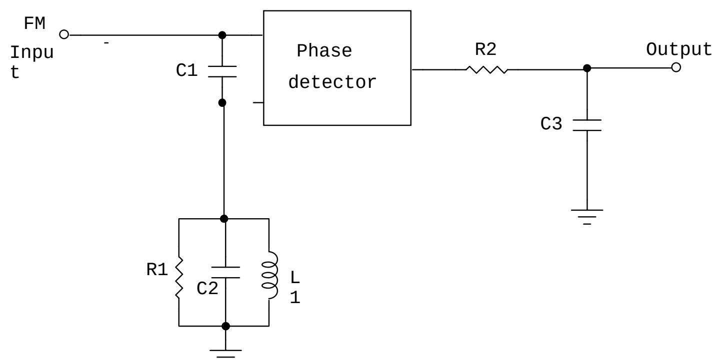


Figure 7 Quadrature detector

The incoming FM input is fed directly to one of the inputs of the phase detector. The same input is also shifted 90^0 by the high reactance capacitor C_1 before being fed to the second input of the phase detector. So the capacitor across the input of the detector makes the signals appearing across the input terminals of the detector to be in quadrature, hence the name quadrature detector. The input signal is also applied to a parallel tuned circuit through capacitor C_1. This cause capacitor C_1 and tuned circuit to work together to convert the frequency changes into phase changes. If the incoming carrier is not modulated, the tuned circuit will be at resonance and will not provide any additional phase shift to the 90^0 that is caused by C_1. However, frequency changes in the incoming FM signal due to modulation will make the tuned circuit to be out of resonance; that is, to be either more inductive or more capacitive thereby resulting in an additional leading or lagging phase shift. This phase shifts are detected by the phase detector to produce a voltage that are proportional to the phase difference between its two inputs. The resultant voltage is averaged by a *RC* low pass filter, formed by R_2 and C_3, to recreate the original modulated signal.

Phase lock loop detector

The last FM detector to be discussed is Phase lock loop (PLL). Unlike other FM detectors already covered in the preceding sections it does not use an inductor. Additional to the elimination of the use of coils, its other advantage is its availability as an integrated circuit, which makes it to be a very cost effective form of demodulator. PLL detector consists of a *phase comparator* or *phase detector*, a low pass filter (LPF), and a *voltage controlled oscillator* (VCO) as shown in Figure 8. However, though it is not shown on the block diagram, commercial PLL linear integrated circuits may have an amplifier to amplify the output of the filter before it is used to drive the VCO or as a demodulated output.

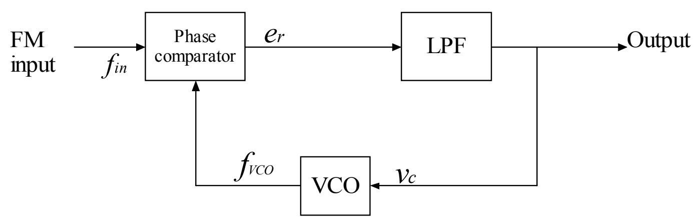


Figure 8 Phase lock loop

The incoming FM signal is fed into the phase comparator together with the output of the VCO and the phase comparator puts out an *error voltage*, e_r, which is proportional to the phase difference between the incoming frequency, f_{in}, and the output frequency of the VCO, f_{co}. The VCO is set such that without any input (i.e. v_c = 0 V), its frequency is equals to the unmodulated carrier of the incoming frequency, which is 10.7 MHz for a FM superheterodyne receiver. However, when modulation takes place, the carrier will deviate and the loop will try to keep the loop in lock. This is done as follows:

- If the received signal is an unmodulated carrier, then frequencies, f_{in}, and f_{co} are equal. Under this condition the output of the phase comparator e_r will be zero volts, therefore the output frequency of the VCO will remain unchanged.
- When the incoming frequency increases above the carrier frequency due to modulation, the phase detector output will also increases above zero. This output voltage will be averaged by the LPF and the averaged voltage will be used to increase the frequency of the VCO to the frequency of the incoming signal.
- When the incoming frequency decreases below the carrier frequency due to modulation, the phase detector output will also decreases below zero. This output voltage will be averaged by the LPF and the averaged voltage will be used to decrease the frequency of the VCO to the frequency of the incoming signal.

These variations in e_r will force the VCO to follow the deviations of the incoming signal. Hence, the control voltage, v_c, at the input of the VCO will be directly proportional to the modulation (deviations) present in the incoming signal. This phenomenon is referred to as *tracking* and when the two frequencies are the same it is said that the VCO is *locked*.

The same voltage that is used to vary the frequency of the VCO is also used as the demodulated output.

A typical IC PLL FM detector using a 560 LIC PLL is shown in Figure 9. The two R_1C_1 network are part of the LPF; C_b is a bypass capacitor; C_d is part of de-emphasis network and the variable capacitor C_o is used to tune the VCO.

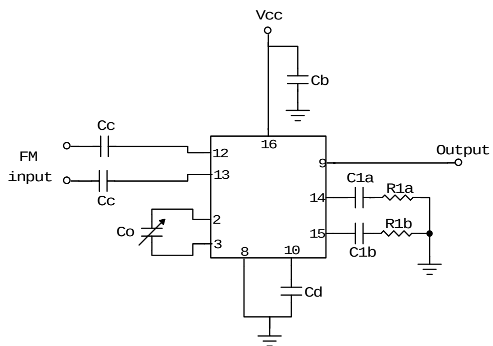


Figure 9 A 560 LIC PLL FM detector

FM stereo demodulation

The receivers discussed so far are used for monophonic broadcast reception; that is, they will reproduce a monaural (mono or L + R) signal at their outputs. However, most of the FM receivers in nowadays are stereo receivers. These receivers are identical to standard superheterodyne receiver up to the detector stage. However, instead of their demodulated outputs being fed to the audio power amplifier, the demodulated composite stereo baseband is fed to a stereo decoder to reproduce the individual left and right channels as shown in Figure 10.

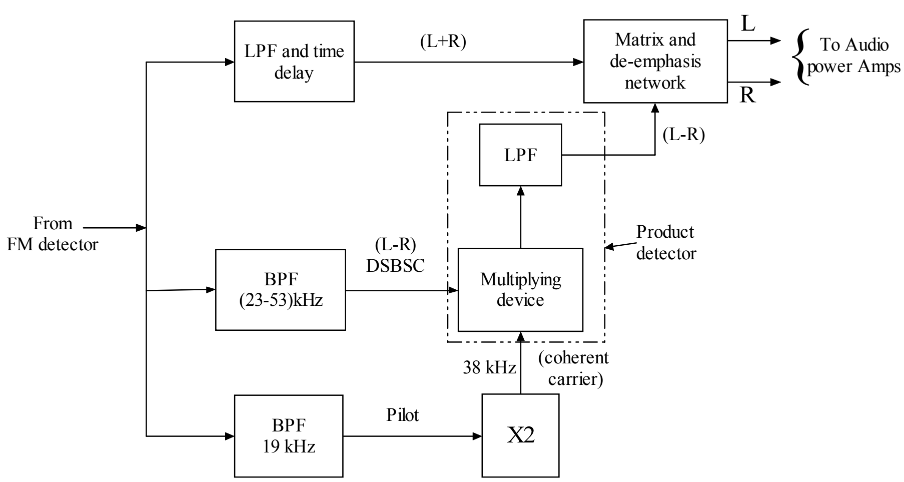


Figure 10 Stereo decoder

The demodulated composite stereo baseband is demultiplexed into three frequency components using three filters; a low pass filter with a high cutoff frequency of 15 kHz and two band pass filters with pass bands of (23 – 53) kHz and 19 kHz, respectively. The three resulting components include the (L + R) signal obtained through a low pass filter, the frequency-translated (L – R) DSBSC signal obtained through a (23 – 53) kHz bandpass filter, and the 19 kHz pilot carrier obtained through a 19 kHz bandpass filter. The (L + R) signal is also given a delay so that it reaches the matrix in step with the demodulated (L – R) signal. The pilot carrier is fed to a *frequency doubler* where it is used to reconstruct the 38 kHz coherent carrier for demodulation. The reconstructed carrier and the frequency-translated (L – R) DSBSC signal are fed to the product detector, which is formed by the multiplying device and the LPF for demodulation. The output of the multiplying device is fed into a low pass filter that will only allow the audio frequency component (L – R) to pass through while attenuating all the other frequency components that are generated by the multiplying device. The (L + R) and the demodulated (L – R) are applied to the matrix network to produce the left and the right channels. Lastly, the resultant left and right channels are de-emphasized before they are fed to the respective audio power amplifiers. A commercially available stereo decoder IC is CA3090.

Quadrature amplitude modulation (QAM) demodulator

Digital radio receivers use quadrature amplitude modulation (QAM) demodulators to demodulate the incoming QAM signals. The block diagram of a QAM demodulator with digital outputs is shown in Figure 11 and that with analogue outputs is shown in Figure 12.

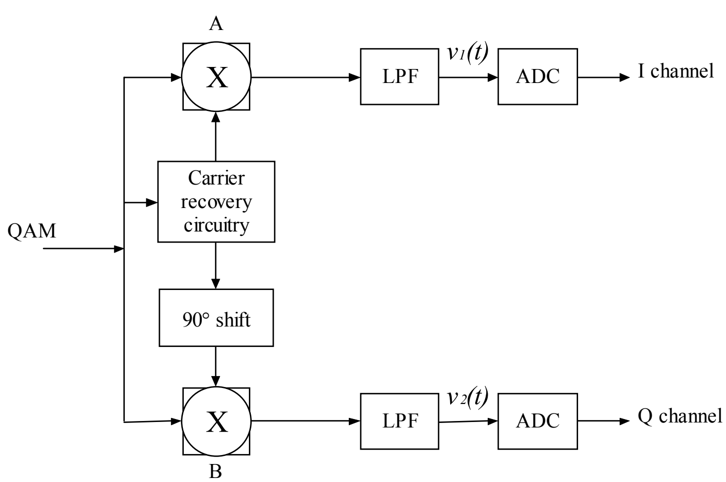


Figure 11 QAM demodulator with digital output signals

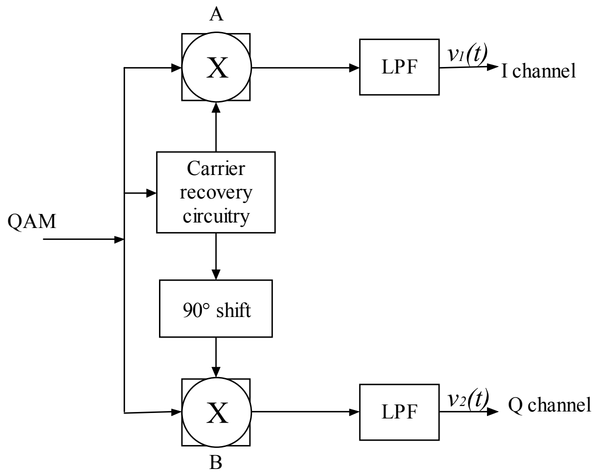


Figure 12 QAM demodulator with analogue output signals

The operation of the two is the same except that the demodulator with analogue outputs does not need to convert the outputs back to digital; hence there are no ADCs after the LPFs.

The incoming QAM signal is fed to two balanced mixers A and B. The carrier that was suppressed at the transmitter is reconstructed from the incoming signal using a carrier recovery circuit. This locally-generated coherent carrier is also applied to the balanced mixers; however, the carrier applied to the balanced mixer B is first phase-shifted by 90^0. The outputs of the mixers are the product of the incoming QAM and carrier signals. Mathematically, the analysis of the QAM demodulator is as follows:

The output of the *I*-channel balanced mixer *A* will be

$$\begin{aligned}
v_{mA} &= v_{QAM} . v_c \\
&= [v_1(t)\sin w_c t + v_2(t)\cos w_c t] \times \cos w_c t \\
&= v_1(t)\sin w_c t \cos w_c t + v_2(t)\cos w_c t \cos w_c t \\
&= \frac{v_1(t)}{2}[\sin(w_c + w_c)t - \sin(w_c - w_c)t] + v_2(t)\cos^2 w_c t \\
&= \frac{v_1(t)}{2}[\sin(2w_c)t - \sin(0)t] + v_2(t)\cos^2 w_c t \\
&= \frac{v_1(t)}{2}\sin 2w_c t - 0 + v_2(t)(1 - \sin^2 w_c t) \\
&= \frac{v_1(t)}{2}\sin 2w_c t + v_2(t) - v_2(t)\sin^2 w_c t
\end{aligned}$$

The output of the *Q*-channel balanced mixer *B* will be

$$\begin{aligned}
v_{mB} &= v_{QAM} . v_{c(Quadrature)} \\
&= [v_1(t)\sin w_c t + v_2(t)\cos w_c t] \times \sin w_c t
\end{aligned}$$

$$= v_1(t)\sin w_c t \sin w_c t + v_2(t)\cos w_c t \sin w_c t$$

$$= v_1(t)\sin^2 w_c t + \frac{v_2(t)}{2}[\sin(w_c + w_c)t - \sin(w_c - w_c)t]$$

$$= v_1(t)\sin^2 w_c t + \frac{v_2(t)}{2}[\sin(2w_c)t - \sin(0)t]$$

$$= v_1(t)(1 - \cos^2 w_c t) + \frac{v_2(t)}{2}\sin 2w_c t - 0$$

$$= v_1(t) - v_1(t)\cos^2 w_c t \frac{v_2(t)}{2}\sin 2w_c t$$

These outputs are fed to low pass filters, which attenuate the second harmonic and square products to allow only the baseband signals $v_1(t)$ and $v_2(t)$ to pass through to the analog-to-digital converters. The analog-to-digital converters are used to convert the analogue signals back to digital so as to obtain *I* and *Q* channel data streams.

Quadrature phase-shift keying (QPSK) demodulator

The block diagram of a coherent QPSK demodulator is as shown in Figure 13 below.

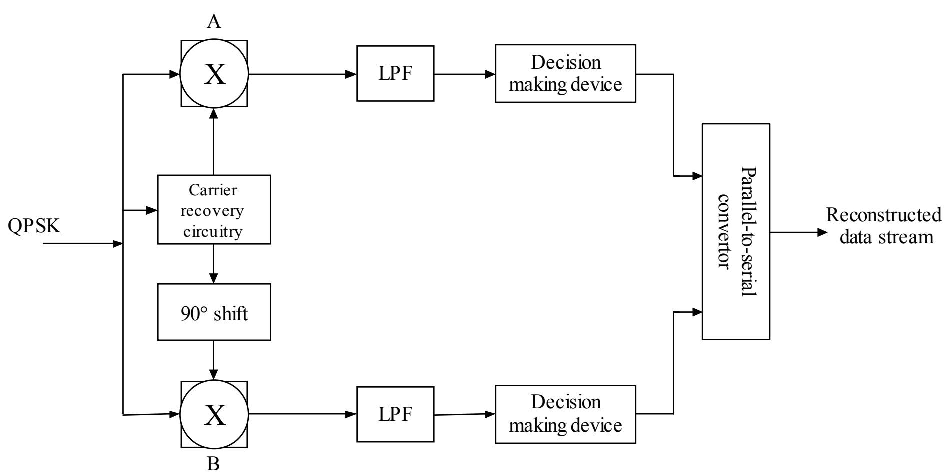


Figure 13 QPSK demodulator

The incoming QPSK signal is fed to two balanced mixers A and B. The carrier that was suppressed at the transmitter is reconstructed from the incoming signal using a carrier recovery circuit. This locally-generated coherent carrier is also applied to the balanced mixers; however, the carrier applied to the balanced mixer B is first phase-shifted by 90^0. The outputs of the mixers are the product of the incoming QPSK and carrier signals. The output of each mixer consists of the original baseband signal and second harmonic products. These outputs are fed to low pass filters, which attenuate the second harmonic products to allow only the baseband signals to pass through to the decision making devices. These decision making devices, which are also known as threshold detectors, usually contain comparators or Schmitt triggers, which use reference threshold values to determine whether a high ('1') or low ('0') is detected. The outputs of the two decision making devices are multiplexed together to reconstruct the original single bit stream using a parallel-to-serial converter.

Gaussian Minimum Shift Keying Demodulation

Demodulation of GMSK signal can be categorized into two: coherent and non-coherent. Figure 14 shows a block diagram of a coherent GMSK demodulator where GMSK is detected by coherently demodulating its inphase and quadrature components separately.

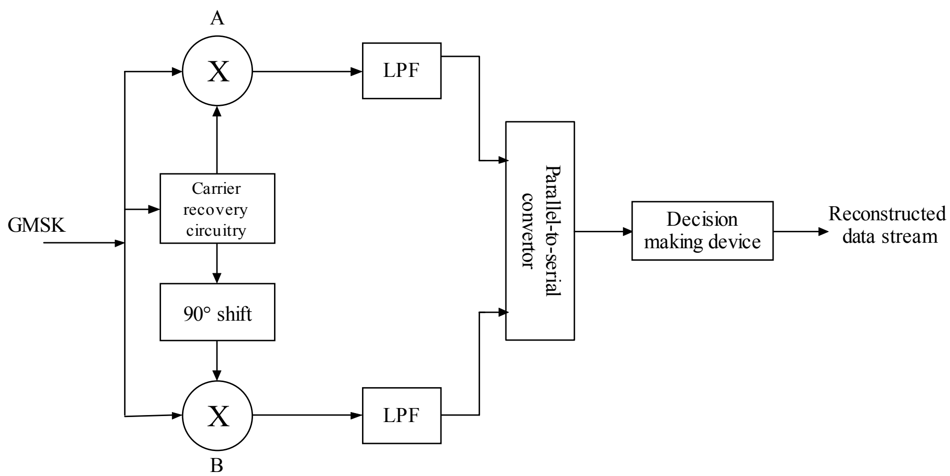


Figure 14 A GMSK coherent demodulator

The incoming GMSK signal is fed to both *I*-channel and *Q*-channel balanced mixers. The carrier that was suppressed at the transmitter is reconstructed from the incoming signal using a carrier recovery circuit. This locally-generated coherent carrier is also applied to the balanced mixers; however, the carrier applied to the balanced mixer B is first phase-shifted by 90^0. The outputs of the mixers are the product of the incoming QPSK and carrier signals. The output of each mixer consists of the original baseband signal and second harmonic products. These outputs are fed to low pass filters, which attenuate the second harmonic products to allow only the baseband signals to pass through to the decision making devices.

Though coherent demodulation is known to perform better than its non-coherent counterpart, it was found that it also degrades in fading environments due to imperfect tracking of the received signal phase which results in irreducible error rates. And under those conditions it was found that non-coherent demodulators perform better. Non-coherent GMSK demodulators do not need the regeneration of the coherent carrier for demodulation in the receiver and they include differential demodulator, the limiter discriminator, and the variations of the two. Figure 15 shows the basic block diagrams for both the differential and limiter discriminator.

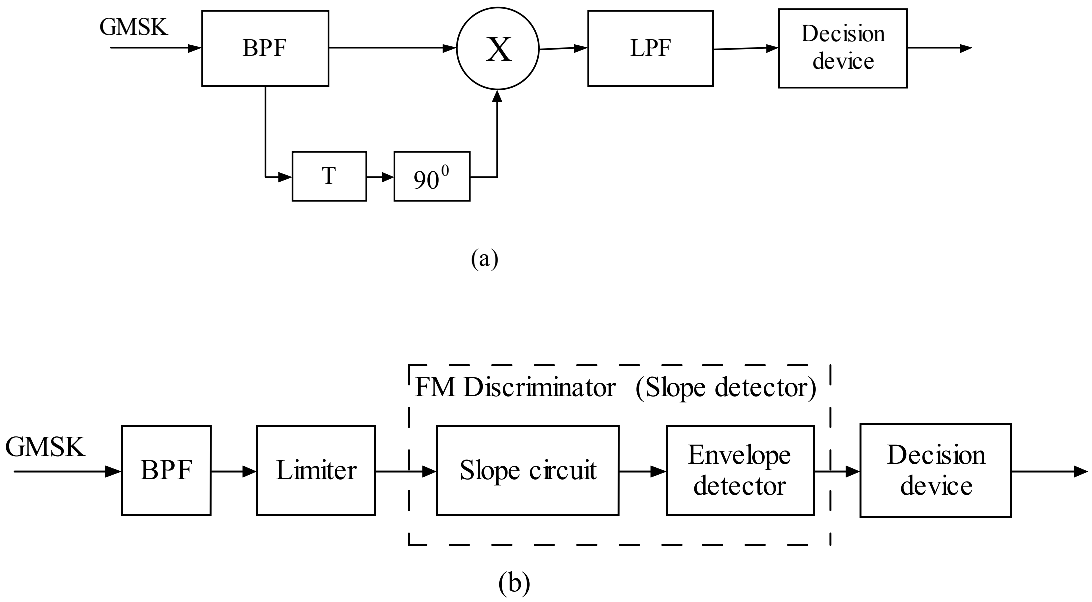


Figure 15 GMSK demodulators: (a) Differential; (b) Limiter discriminator

GMSK uses a modulation index of 0.5, which limits the phase change in the resultant GMSK to less than π/2 (or 90^0) within any two bits. The direction of change depends on the actual symbol being transmitted. In differential demodulation the phase change over one bit is extracted

In a Limiter discriminator the incoming GMSK signal is first filtered using a band pass filter. The filtered signal is then passed through a limiter to restore a constant envelope property to the corrupted received signal. The output of the limiter is applied to a slope detector, which is a FM discriminator, that consists of a slope circuit and an envelope detector. The slope circuit extracts the instantaneous frequency deviation of the GMSK signal and converts them to corresponding amplitude variations; that is, it converts the frequency modulated GMSK signal into an amplitude modulated signal. The amplitude variations are then detected by the envelope detector. The output of the envelope detector is usually averaged before it is fed to a decision making devices or threshold detectors, which usually contain comparators or Schmitt triggers that use reference threshold values to determine whether a high ('1') or low ('0') is detected.

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